	Class: VME		Function: Optical to RF (DIGITAL)	
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RF_RX_D v2.0

SIMPLIFIED USER MANUAL
-VME MAPPING-

Summary:

This document describes the VME mapping of the RF_Rx_Digital Board. For more information about hardware, see the hardware user manual.

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1. INTRODUCTION

The RF_RX_D (Optical to RF VMEbus card) is an interface VME card developed as receiver of RF_TX_D VMEbus Interface card.

This document contains a description of the accessible registers of the RF_RX_D board.

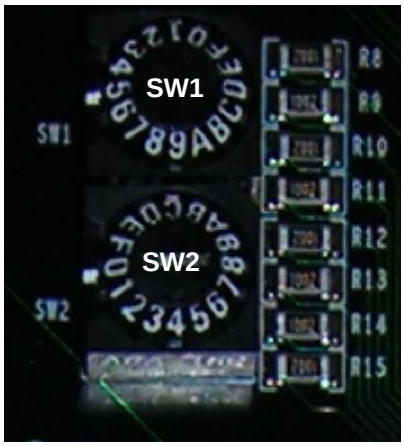
For more details about the various hardware flavours of the RF_Rx, see the complete user manual.

2.2. VMEBUS INTERFACE

The VMEbus interface of the RF_RX_D cards is implemented in its FPGA and based on a VHDL Module developed by the AB/RF group. This Module has been developed especially for VME64 but adapted for using some functionality of VME64X (like automatic addressing).

The firmware installed has been configured to work in the addressing mode of: A24/D16 and works as a memory decoder, where all the memory space is available.

The access modes (dictated by address modifier) are only available for 0x39 and 0x3D, where the there is no distinction between privilege user and normal user



Picture 2.3: Module address selector

Two switches are used for address definition:

SW1: only the smallest bit is used.

If bit0 is set to 0 (SW1= 0x0, 0x2, 0x4, 0x6…), the SW2 defines the address.

if bit 0 is set to 1 (SW1= 0x1, 0x3, 0x5 …), the address is set by the geographical position of the module in the crate.

2.3.1. ADDR MODULE SELLECTION

Rotary Switch 1 (bit0)	Rotary Switch 2	Module address (MA)
1	M	Automatic GEO Address [A23…A20] <= GEOGA(3 : 0)
0	M	0xM Manual Address [A23…A20] <= M

**Requires VME64X crate*

Table 2.3.1: Address and ADDR Mode selection

In others words, the bottom rotary switch (sw1) controls the addressing mode with the lower two bits, which switches to automatic mode if the bit(0) or bit(1) = 1.

Examples:

Rotary Switch 1	Rotary Switch 2	Module MODO / ADDRESS / SPACE
0x1	5	Manual address Module address: 0x50 0000
0x0	X	Geographical address Module address: Depends on the slot into which the card is plugged
0x3	4	Manual address Module address: 0x40 0000

Table2.3.1.b: Examples of Module Addr

2.3.2. SOFTWARE: VME ADDRES MAP

Offset	Size (bytes)	Function	Mode	Remarks
0xN00000	2	Unused		
0xN00002	2	VMEIRQStatID	Read / Write	
0xN00004	2	VMEIRQLevel	Read / Write	
0xN00006	2	Status	Read Only	
0xN00008	2	Ident Code	Read Only	0x001A
0xN0000A	4	Unused		
0xN00010	2	ReceiverModID	Read Only	Note (1)
0xN00012	2	CH1_OUTPUT_REF_SIGNAL	Read / Write	TRR module only, Def. Val. 0xA0
0xN00014	2	CH2_OUTPUT_REF_SIGNAL	Read / Write	TRR module only, Def. Val. 0xA0
0xN00016	2	CH3_OUTPUT_REF_SIGNAL	Read / Write	TRR module only, Def. Val. 0xA0
0xN00018	4	CH1_FREQ	Read Only	Freq Ch1 (0..31), Note (2)
0xN0001C	4	CH2_FREQ	Read Only	Freq Ch2 (0..31), Note (2)
0xN00020	4	CH3_FREQ	Read Only	Freq Ch3 (0..31), Note (2)
0xN00024	2	CARD ID	Read Only	0x1382
0xN00026	2	unused		
0xN0003A	2	BOARD ID	Read Only	0x016C
0xN0003C	180	Unused		Unused
0xN000F0	4	FirmwareVer	Read Only	Firmware version
0xN000F4		Unused		
0xN50000	64 kbyte	CTRV VME Slot 1		Reserved
0xN60000	64 kbyte	CTRV VME Slot 2		Reserved
0xN70000	64 kbyte	CTRV VME Slot 3		Reserved
>0xN80000		Unused		Unused

2.3.3. REGISTERS DESCRIPTION

2.3.3.1. RECEIVERMODID

Bits 0-5 of the Receiver Module Ident code word are used to identify the installed Receiver modules (between OCP SRX03 or SRX24, and TRR)

ReceiverModID		0xN00006
bit	**Function**	**Remarks**
0-1	Ch1	See below
2-3	Ch2	See below
4-5	Ch3	See below
6-15	Unused	

The two-bit code has the following meaning:
00 = No module installed
01 = OCP SRX03
10 = OCP SRX24
11 = TRR, Truelight Module

2.3.1.1. STATUS

Name	Offset	Size	Access	Default Values
STATUS	0x006	8 bits	R/W	0xA0

Bits	Function	Remarks
STATUS	0x006	8 bits
15-3	Unused	
2	PrstCh3	1 = CH3 present*
1	PrstCh2	1 = CH2 present*
0	PrstCh1	1 = CH1 present*

The channel is declared as being present if the measured frequency (see CHX_FREQ registers) matches with the following table:

	frequency
OCP	8.99 MHz up to 402.28 MHz
TRR	1.6 kHz up to 50.01 MHz

OCP :SRX03 & OCP SRX24

TRR : Truelight Module

2.3.3.2. VREF REGISTERS (ONLY FOR TRR OR EQUIVALENT PHOTODIODES)

These registers only work with the photodiodes plugged in the Truelight socket. They set up the value of the comparator threshold installed at the input of each channel. For a balanced signal (typically a clock), the value must be as low as possible, but has to be above the noise threshold.

Name	Offset	Size	Access	Default Values
CH1_OUTPUT_REF_SIGNAL	0x0012	8 bits	R/W	0xA0
CH2_OUTPUT_REF_SIGNAL	0x0014	8 bits	R/W	0xA0
CH3_OUTPUT_REF_SIGNAL	0x0016	8 bits	R/W	0xA0

For a balanced signal (typically a clock), the value must be as low as possible, but has to be above the noise threshold. That is why the appropriated value for clock signals is between 0x05 and 0x09 at -12dB.

For a unbalanced signal (typically a pulse (Revolution Frequency, injection pulse)), the value must be more than the amplitude of the pulse at the output of the optical receiver, but not too high. That is why the appropriated value for pulse signals is between 0x70 and 0xA0 at -12dB.

For more details, see the detailed user manual.

Note: be careful, if the VREF value is 0x0 (see below), the module is measuring the frequency of the noise…And it is possible that the measured frequency of the picked up noise recognised as a good one. So never put less than 0x5 on the VREF registers

2.3.3.3. FREQUENCY COUNTERS

CH1

Name	Offset	Size	Access
CH1_FREQ_LOW	0x0018	16 bits	R
CH1_FREQ_HIGH	0x001A	16 bits	R

CH2

Name	Offset	Size	Access
CH2_FREQ_LOW	0x001C	16 bits	R
CH2_FREQ_HIGH	0x001E	16 bits	R

CH3

Name	Offset	Size	Access
CH3_FREQ_LOW	0x0020	16 bits	R
CH3_FREQ_HIGH	0x0022	16 bits	R

The full 32 bits frequency register must be read in a special order. Which is from LSW to MSW.

If not the 32 bits register won't be updated the right way.

These registers are generated by internal counters that count the number of rising clocks between rising edges in the received signals.

In order to measure higher frequencies than the clock frequency, a frequency divider has been installed on the board (4 hardware Flips-Flops = > 1/16) and inside the FPGA (software divider 1/22)

Every counter has a size of 32 bits that is divided in two registers of 16bits that must be read separately due to the fact that the board has only A24/D16 access.

In order to calculate the frequency, the equation is:

$$Freq = \frac{80 \bullet 16 \bullet 22}{FreqLow + FreqHigh \bullet 65536^{*}}$$

* This multiplication must be done in LONG UNSIGNED INT or FLOAT

Examples:

Frequency Original (MHz)	ValueReg1	Value Reg2	Frequency Measured (MHz)
10	0x0000	0x0B00	10
40.078	0x0000	0x02BF	40.0568
	0x0000	0x02BE	40.113
400.78	0x0000	0x0047	396.619
	0x0000	0x0046	402.285
Pulse 1MHz	0x0000	0x6e00	1MHz
Pulse 11.245KHz	0x0026	0x361A	11.245027KHz
No signal	0xFFFF	0xFFFF	6Hz

Table 2.3.3.4 : Typical examples of values of the frequency counter

2.3.3.4. BOARD IDENTIFICATION

2.3.1.2. IDENT CODE

Ident Code			0xN0008
Bit	Function	default	access
0-15	Ident Code	0x1A	R

2.3.1.3. CARD ID

CARD ID			0xN00024
Bit	Function	default	access
0-15	CARD ID	0x1382	R

This register contains the EDA number of the board (EDA-001382)

2.3.1.4. BOARD ID

BOARD ID			0xN0003A
Bit	Function		access
0-15	BOARD id	0x016C	R

This register contains the VME64x board ID of the RF-RX (CERN centrally defined) and is set to the value 364 (0x16C). See http://ess.web.cern.ch/ESS/boardIDistribution/PHP/ for details

2.3.1.5. FIRMWARE VERSION

Firmware version			0xN0003A
Bit	Function		access
0-31	Firmware version		R