TTC RECEIVER CRATE

SPECIFICATIONS

Draft

Sophie Baron
PH-ESS
- 28 November 2005 -

Table of contents

1 INTRODUCTION

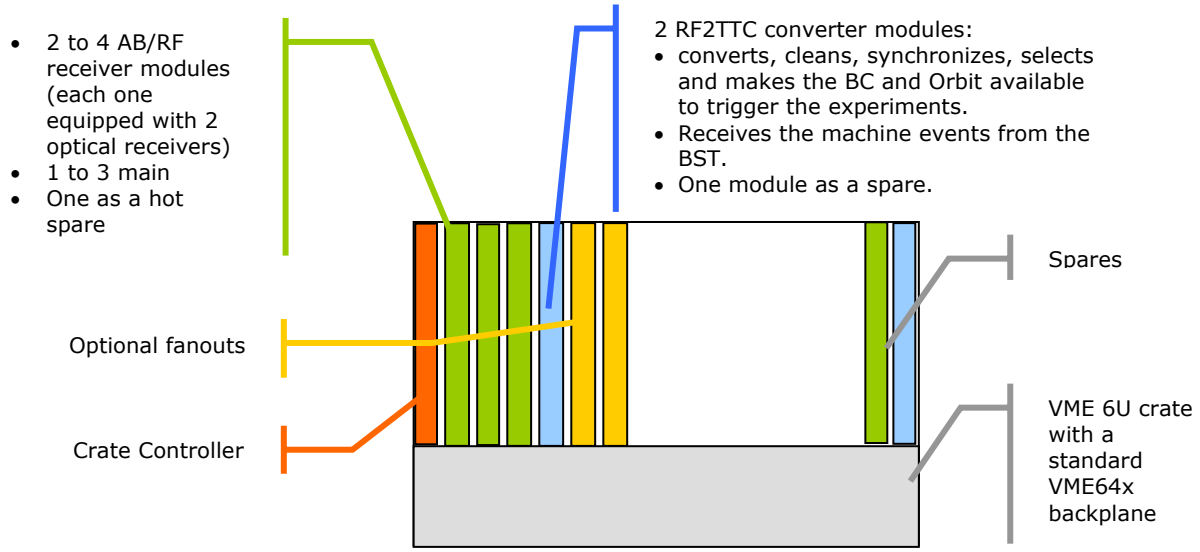
The TTC receiving crate is part of the project of upgrading the TTC backbone system, described in: https://edms.cern.ch/file/628545/2/TTC_system_upgrade.pdf.

Its task is to replace the TTCmi, receiving the RF timing signals, preparing them for being used by the experiments, and allowing a remote control and monitoring of the main functionalities.

2 CRATE DESCRIPTION

2.1 Equipment description in experimental areas

The equipment necessary to receive, convert, clean and transmit the BC and Frev signals will be the same in each experiment and is as described below:



The minimum equipment to be installed in each experiment consists of:

- One standard VME crate (6U VME64x). The ALICE crate will probably be water cooled due to the ambient magnetic field (200 gauss);
- One crate controller (a Single Board Computer type VP110 from Concurrent Technologies is recommended but could be replaced by another type of controller if required by the experiment);
- 2 AB/RF receiver 6U VME modules, housing 2 optical receivers, complementary to the transmitters previously described. Each module will deliver 2 analog signals (either BC or Orbit) to the RF2TTC module via SMA connectors. The probable scheme is 4 AB/RF standard receiver modules per experiment (3 receiving the main BC and Frev signals, and one as a spare module);
- 2 TTC2RF interface boards (one main and one spare).

Each experiment will provide a place to install this receiver crate. One complete system will also be installed in the TTC lab in building 4.

2.2 Location

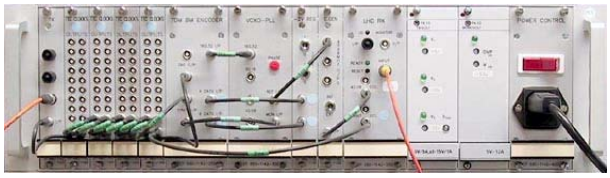
5 receiver crates will be installed. One in each experiment, and one for development and support, in the TTC lab (4-R-029).

	Local
ALICE	RB26
ATLAS	USA15, level-1
CMS	USC55
LHCb	2828-UX85
TTClab	4-R-029

3 CRATE FUNCTIONALITIES

As the previously described VME crate, including the RF2TTC module, will replace 3 previous TTCmi minicrates, it has at least to provide the same functionalities.

3.1 Previous TTCmi



The main document describing the TTCmi can be found at:
http://www.cern.ch/TTC/TTCmiManual.pdf
Global information can be also found on the TTC website:
http://ttc.web.cern.ch/TTC/intro.html => TTC machine interface

3.2 Compared functionalities

	TTCmi			New system		
	Functionality	Provided by	Comments	Provided by	Comments	
Reception	Optical level adjustment	Optical attenuator		RF attenuator for CMS	And a comparator at the input of the RF2TTC module	
	Optical reception of encoded BC and Orbit	LHCrx	optoelectrical conversion + amplification	AB/RF Rx	BC and Orbit on separate fibres. Transmitted via SMA connector to the RF2TTC module.	
	Decoding	LHCrx		-	No decoding required, but a phase adjustment of the orbit to tune the synchronization. Done by RF2TTC module	
Internal features	Internal 40.078MHz clock	C. Gen		RF2TTC	QPLL in stand alone mode	
	Switch between external and internal clock (manual)	C. Gen		RF2TTC	Remotely controlled by a VME register.	
	Orbit digital phase adjustment (manual)	LHCrx	3564 steps of 25ns	RF2TTC	Remotely adjustable by a VME register. Done in the FPGA	
	Orbit pulse stretcher to 1us (fixed)	LHCrx		RF2TTC	Remotely adjustable by a VME register. Done in the FPGA	
	BC cleaning (PLL with VCXO)	VCXO-PLL	BC jitter = 7ps rms ensured by a very stable VCXO	RF2TTC	Done by a QPLL	
Out	Orbit output / ECL			RF2TTC	2 outputs types (ECL and NIM)	
	BC output / ECL			RF2TTC	2 outputs types (ECL and NIM)	
Monitoring	Optoelectrical conversion for signal monitoring with a scope (local)	LHCrx	Physical ECL AC coupled output. Needs a separate optical input.	AB/RF Rx	Lemo output on AB/RF module front panel. (NIM?). Scope (local) monitoring.	
	TTCrx ready (local)	LHCrx	Led	RF2TTC	QPLL lock monitoring and Orbit detection flag. Remotely monitored	
	Presence of optical signal at a correct power level (local)		Led	AB/RF	Optical power monitored by AB/RF.	
Options	Orbit fanout / ECL	TTCcf	optional	TTC Fanout		
	BC fanout / ECL	TTCff	Optional – typical jitter values at the output = 10ps rms	TTC Fanout		
	TDM&BM encoding	TDM BM Encoder	optional	TTCex		
	Optical fanout	TTCmx	optional	TTCex/tx		

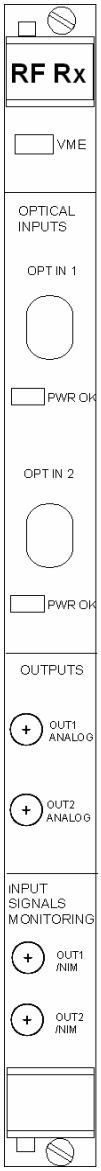
3.3 New functionalities

New functionalities	Provided by	
BC phase adjustment	RF2TTC	Not necessary in the previous system. Required to ensure a good synchronisation
Automatic clock switch	RF2TTC	Automatic mode to switch at injection and beam dump. Can be disabled by VME access.
Main BC source selection	RF2TTC	Controlled by VME access. Select BC output between BC ring1, BC ring2, BC ref and Internal BC
Main Orbit source selection	RF2TTC	Controlled by VME access. Select Orbit output between Orbit ring1, Orbit ring2,
Clock and Orbit ECL outputs driven by a 25 Ohms line driver.	RF2TTC, Fanout	

4 MODULE SPECIFICATIONS

4.1 Crate controller

4.2 AB/RF receiver module



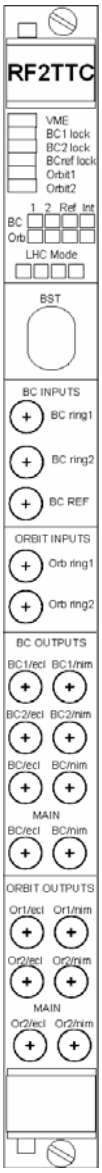
This is a very preliminary view of the AB/RF Receiver module. This module will ensure the reception of 2 analog signals from the RF. The receiver modules will very likely be MITEQ receivers.
The specifications of this module will be defined by the AB/RF group. The design will be done by the PH/ESS group, in close collaboration to the AB/RF group, and using their VHDL library for the VME interface.

The analog outputs will be used by various types of customers:

- AB/RF electronics at SR4
- AB/CO and BDI electronics at CCC
- RF Tx modules at CCC
- RF2TTC modules at the experiments

4.3 RF2TTC module

This is a very preliminary overview of the front panel of the RF2TTC module, showing local monitoring diodes, inputs and outputs. They are detailed in the following sections, as well as the functionalities. The Front panel may be made on a 2 slots wide size if requested. (like the ATLAS LTP for example).



4.3.1 Inputs

Two types of inputs have to be available on the RF2TTC Front Panel:

- BST (optical ST/PC connector of a TRR photodiode receiver and amplifier)
- 5 RF timing signals (Lemo or SMA).

The RF timing inputs are directly taken from the RF Rx modules. As 3 BC types and 2 Orbit types can be delivered by these modules, 5 inputs are foreseen in the front panel. To simplify, 'Orbit' is used for Frev or Orbit indistinctively.

Question:

- *connector types: SMA or Lemo connectors?*

The signals are analog, and their amplitude varies with respect to the optical link attenuation (cf. RF Rx section).
The signals are estimated to be:

- BC: ~-5dBm (sinusoidal, 50 Ohms)
- Orbit: .5V pkpk (one sinusoidal pulse, 5ns width)

4.3.2 Outputs

It is proposed to provide 1 pair of ECL and NIM outputs per input, plus one pair of MAIN BC (ECL and NIM) and MAIN ORBIT (ECL and NIM). The connect ors used for the outputs will be Lemos.

The direct pairs of BC are just simply the converted inputs, cleaned by a QPLL.
Questions:

- *Should we multiplex them with the internal clock?*
- *Should we be able to adjust the phase of each BC out?*

The MAIN BC is multiplexed between BC1, BC2, BCref and Internal BC. The multiplexer is controlled, either by VME access, or automatically, using the machine modes delivered by the BST. This selected clock is then phase adjusted and cleaned by a QPLL. It is used to latch the orbit signal.

Question:

- *Should we have a separated output for the MAIN BC, or can we use the 3rd BC output pair (BC ref) to ensure this functionality?*

The direct pairs of Orbit are synchronized to the MAIN BC and stretched with an adjustable length. To ensure a stable synchronization, the input orbit phases are also adjustable.

The MAIN ORBIT is multiplexed between Orb1, Orb2 and an adjustable internal counter running at the MAIN BC frequency.
Question:

- *Should we have a separated output for the MAIN ORBIT, or can we simply multiplex each orbit (between the real and the internally generated) before going to output?*

4.3.3 Control functions

The following functions can be controlled by VME access:

- BC signals:
  - Phase adjustment (I2C control via fpga/VME) of each output (each?)
  - For the 3 BCs, selection between internal clock and external input from RF Rx module (or not?)
  - Global selection for the MAIN BC output, between BC1, BC2, BCref and BCint
  - Automatic switching mode for the Main BC selection (using the LHC mode transmitted by the BST)
- Orbit signals:
  - Phase adjustment for synchronisation with the Main BC.
  - Pulse width adjustment
  - Switch between internal counter and Frev input from the RF Rx module
  - Reference voltage adjustment (DAC) for the Orbit comparator
- Internal clock tuning (if the QPLL is used, it is possible to slightly tune the frequency)

Question:

- *Would 500ps steps be enough for BC phase adjustment (in that case, we can use the delay25 chip, which has a range of 25ns)?*

Note: as the BC is a DC balanced signal, no voltage adjustment should be required for the BC comparator used as a receiver. The GND will be used as a reference voltage.

4.3.4 Monitoring functions

The module proposes 2 types of monitoring:

- Local monitoring:
  - LEDs: BCs lock, Orbit present, VME access, selected signals for Main Orbit and Main BC, LHC mode
  - Scope: each ECL output is duplicated with a NIM output
- Remote monitoring (via VME registers):
  - All the adjustment parameters previously described can of course be read back
  - QPLL lock and error signals
  - LHC modes (decoded from the BST signals)

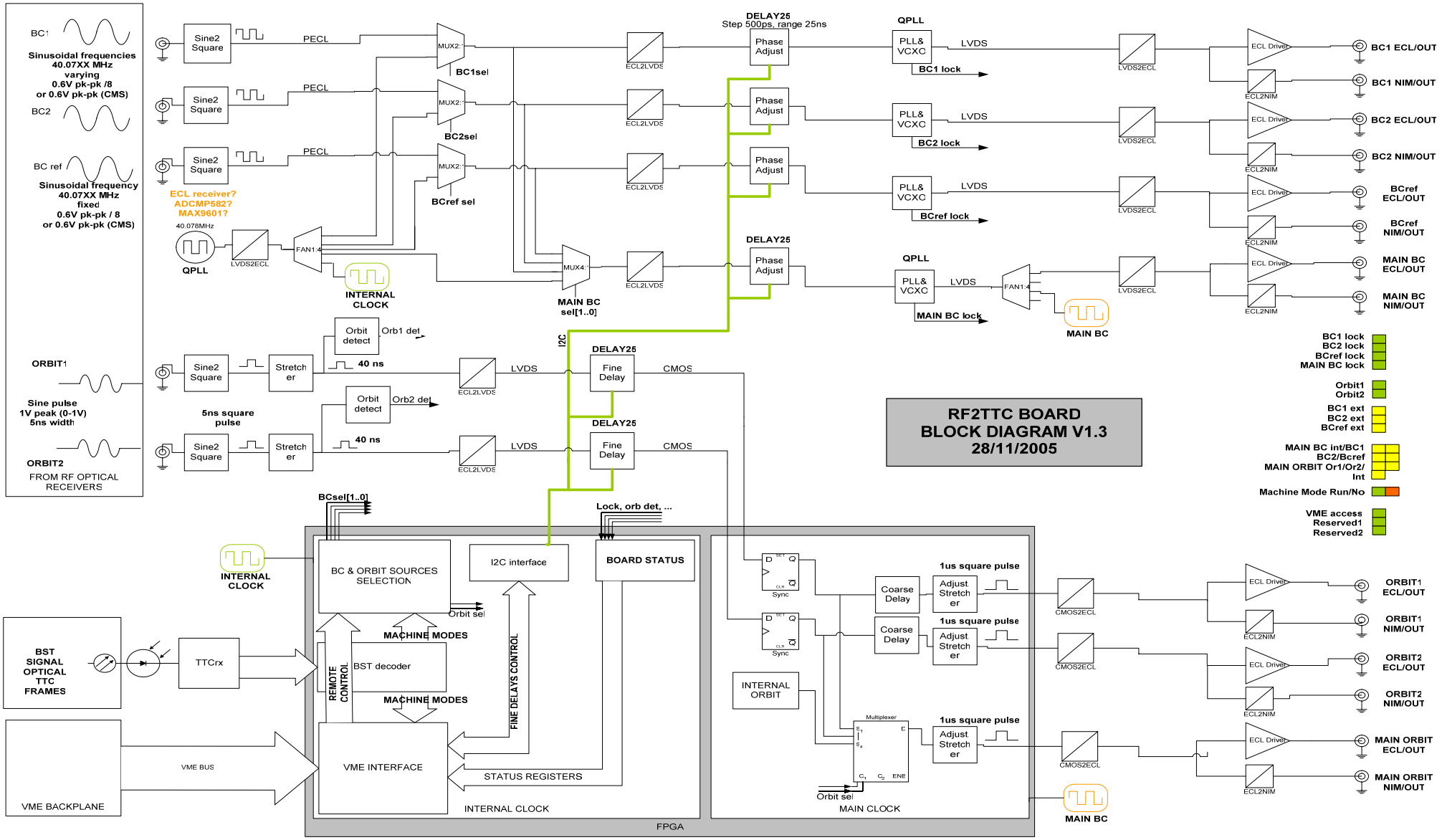
5 RF2TTC TECHNICAL SOLUTIONS

The module form factor will be 6UVME. The front panel may be 2 slots wide due to the number of connectors required.

5.1 Special components (preliminary)

- BC reception: Analog Device AD96685 or ADCMP561
- Orbit reception: Analog Device AD96685 or ADCMP561, biased with a reference voltage provided by a DAC from Maxim (MAX505 for example).
- Phase adjustment: Delay25 chips, controlled by I2C bus
- PLL & Internal clock generator: QPLL + 160.32MHz Quartz from Microcrystal
- ECL line drivers: MC100EL12

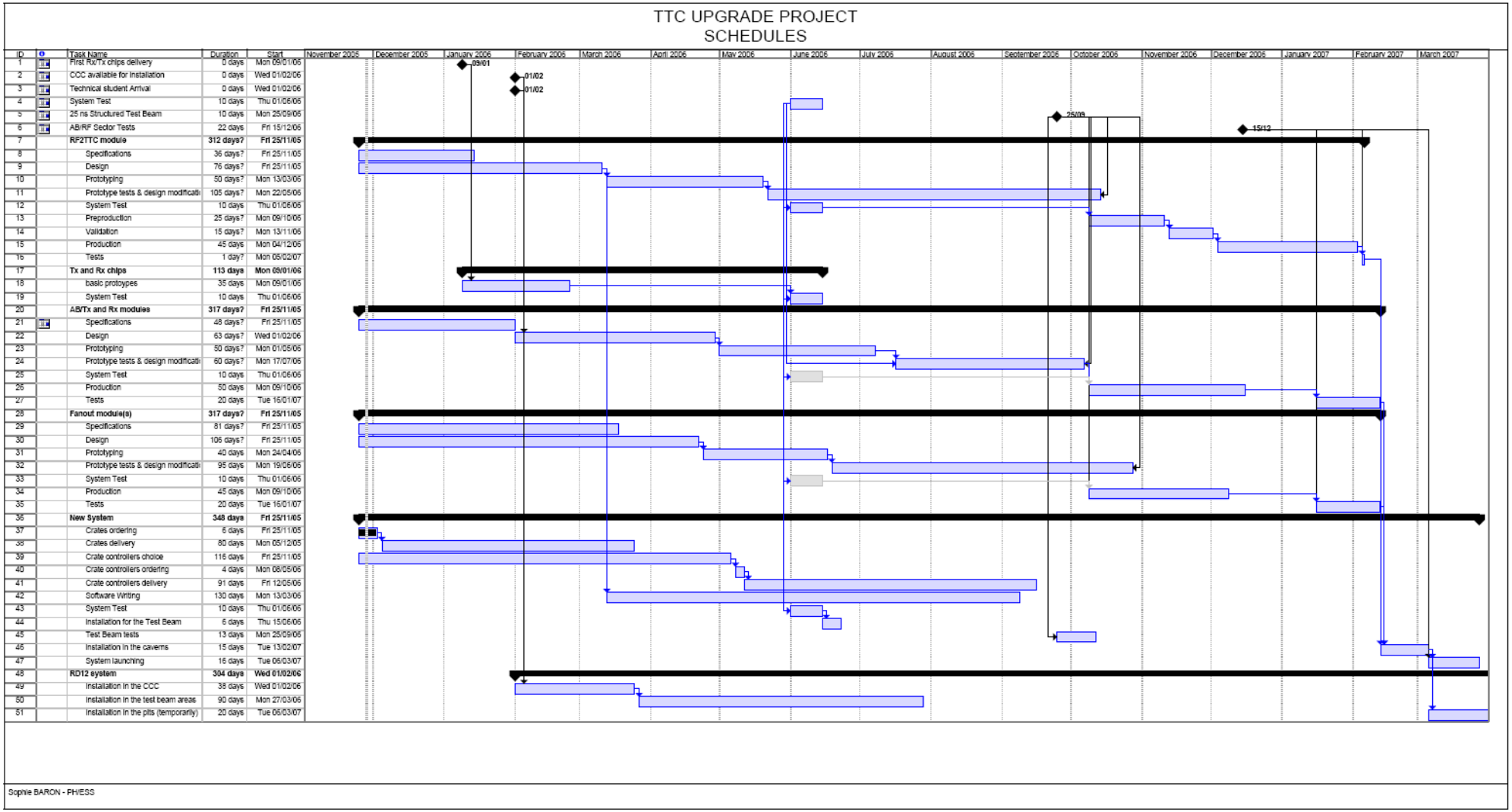
5.2 Block diagram (preliminary)



6 SCHEDULES

Various modules will be designed at the same time. The main milestones are the following:

- beginning of 2007: all the systems are installed in the pits,
- September 2006: 25ns structured test beam,
- End of Spring 2006: first prototypes ready,
- January 2006: first optical transmitters and receivers available (10 have been ordered by the AB/RF).



ID	Task Name	Duration	Start
1	First Rx/Tx chips delivery	0 days	Mon 09/01/06
2	CCC available for installation	0 days	Wed 01/02/06
3	Technical student Arrival	0 days	Wed 01/02/06
4	System Test	10 days	Thu 01/06/06
5	25 ns Structured Test Beam	10 days	Mon 25/09/06
6	AB/RF Sector Tests	22 days	Fri 15/12/06
7	**RF2TTC module**	**312 days?**	**Fri 25/11/05**
8	Specifications	36 days?	Fri 25/11/05
9	Design	76 days?	Fri 25/11/05
10	Prototyping	50 days?	Mon 13/03/06
11	Prototype tests & design modificati	105 days?	Mon 22/05/06
12	System Test	10 days	Thu 01/06/06
13	Preproduction	25 days?	Mon 09/10/06
14	Validation	15 days?	Mon 13/11/06
15	Production	45 days	Mon 04/12/06
16	Tests	1 day?	Mon 05/02/07
17	**Tx and Rx chips**	**113 days**	**Mon 09/01/06**
18	basic protoypes	35 days	Mon 09/01/06
19	System Test	10 days	Thu 01/06/06
20	**AB/Tx and Rx modules**	**317 days?**	**Fri 25/11/05**
21	Specifications	48 days?	Fri 25/11/05
22	Design	63 days?	Wed 01/02/06
23	Prototyping	50 days?	Mon 01/05/06
24	Prototype tests & design modificati	60 days?	Mon 17/07/06
25	System Test	10 days	Thu 01/06/06
26	Production	50 days	Mon 09/10/06
27	Tests	20 days	Tue 16/01/07
28	**Fanout module(s)**	**317 days?**	**Fri 25/11/05**
29	Specifications	81 days?	Fri 25/11/05
30	Design	106 days?	Fri 25/11/05
31	Prototyping	40 days	Mon 24/04/06
32	Prototype tests & design modificati	95 days	Mon 19/06/06
33	System Test	10 days	Thu 01/06/06
34	Production	45 days	Mon 09/10/06
35	Tests	20 days	Tue 16/01/07
36	**New System**	**348 days**	**Fri 25/11/05**
37	Crates ordering	6 days	Fri 25/11/05
38	Crates delivery	80 days	Mon 05/12/05
39	Crate controllers choice	116 days	Fri 25/11/05
40	Crate controllers ordering	4 days	Mon 08/05/06
41	Crate controllers delivery	91 days	Fri 12/05/06
42	Software Writing	130 days	Mon 13/03/06
43	System Test	10 days	Thu 01/06/06
44	Installation for the Test Beam	6 days	Thu 15/06/06
45	Test Beam tests	13 days	Mon 25/09/06
46	Installation in the caverns	15 days	Tue 13/02/07
47	System launching	16 days	Tue 06/03/07
48	**RD12 system**	**304 days**	**Wed 01/02/06**
49	Installation in the CCC	38 days	Wed 01/02/06
50	Installation in the test beam areas	90 days	Mon 27/03/06
51	Installation in the pits (temporarily)	20 days	Tue 06/03/07