EDA-01357
SpecctraQuest Analysis

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IT/DES

Analysis Overview

- Problem
  - Extra amount of jitter has been previously measured on the path corresponding to BCRef (the first appearance of extra jitter is noticed at the Delay25 chip)
- Strategy
  - As the PCB layout is done with Cadence Allegro we have used SpecctraQuest to simulate/analyse the existing board
  - Use SQ to extract the topology (transmission lines, vias and test points models)
  - Perform time-domain simulation and compare the results (from SI point of view) for the path corresponding to BC1, BC2 and BCRef
- Limitations
  - SpecctraQuest (SQ) simulations are point-to-point, so the transmission channel can be only analysed partially from one chip to the other
  - Not all the chip have available IBIS models so not all paths can be analysed either
- Objective
  - Is it any difference between the paths for BC1, BC2 and BCRef

  ➔ can we detect a problem on the board ?

Analysis Details

The following paths (point-to point connections) have been analysed:

- MC100LVEL11 = Interconnect = DELAY25

  for BC1, BC2 and BCRef (slide 3/4/5)

  ➔ can we see any difference between BC1-BC2-BCRef ?
- MC100LVEL11 = Interconnect = MC100EP57(IC48) **AND** MC100EP57 = Interconnect = Delay25 (slide 6/7)

  ➔ how does the signal look like at the receiver ?
- MC100EP56 = Interconnect = MC100LVEL11 for BC2 and BCRef (slide 9)

  ➔ can we see any difference between BC2-BCRef ?

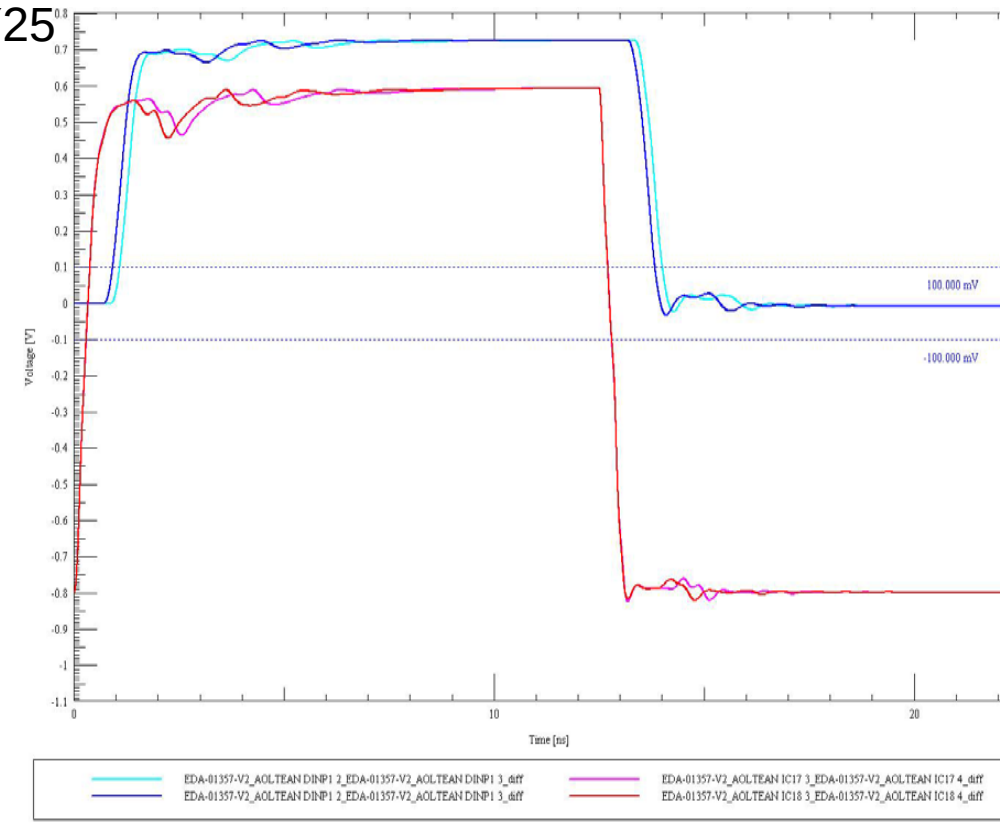
MC100LVEL11 = Interconnect = DELAY25
BC1 compared to BC2 [1]

Simulated path
MC100LVEL11 = Interconnect = DELAY25

BC1
MC100LVEL11 (IC18.3 | 4)
DELAY25 (IC54.31 | 32)
TP: 39, 41, 49, 52

BC2
MC100LVEL11 (IC17.3 | 4)
DELAY25 (IC54.29 | 30)
TP: 18, 20, 30, 31

Comments
- Models used:
  - -IBIS for MC100LVEL11
  - -IBIS Default for DELAY25



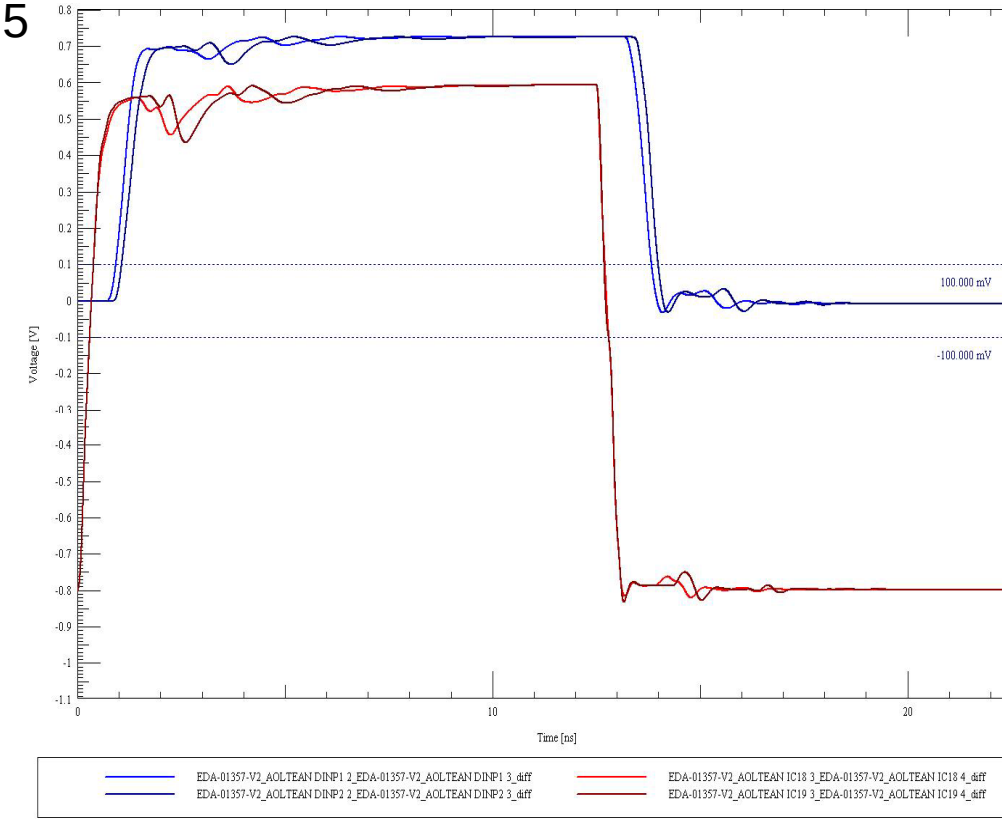
➔ can we see any difference between BC1-BC2?
No, not really!

MC100LVEL11 = Interconnect = DELAY25
BC1 compared to BCRef [2]

Simulated path
MC100LVEL11 = Interconnect = DELAY25

BC1
MC100LVEL11 (IC18.3 | 4)
DELAY25 (IC54.31 | 32)
TP: 39, 41, 49, 52

BCRef
MC100LVEL11 (IC19.3 | 4)
DELAY25 (IC54.27 | 28)
TP: 22, 24, 32, 33



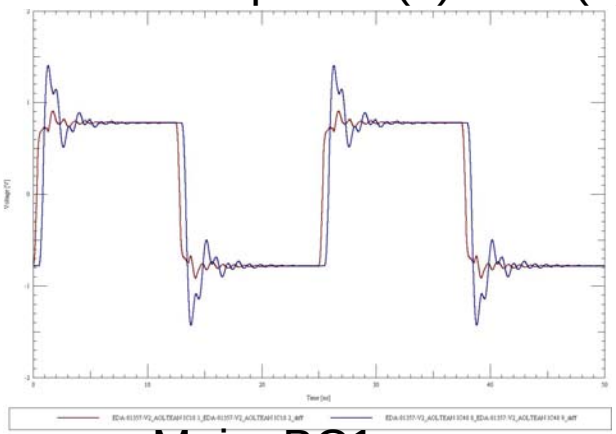
➔ can we see any difference between BC1-BC2?
No, not really! The waveforms for BC1, BC2 and BCRef look very similar!

MC100LVEL11 = Interconnect = MC100EP57(IC48)
BC1 | BCRef | BC2 [1]

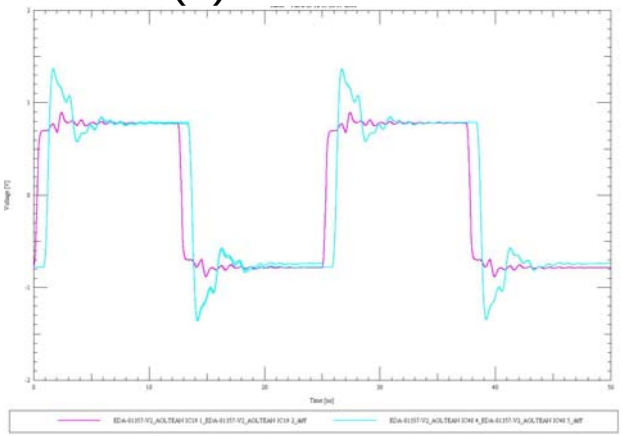
Simulated path

MC100LVEL11 = Interconnect = MC100EP57 (IC48)

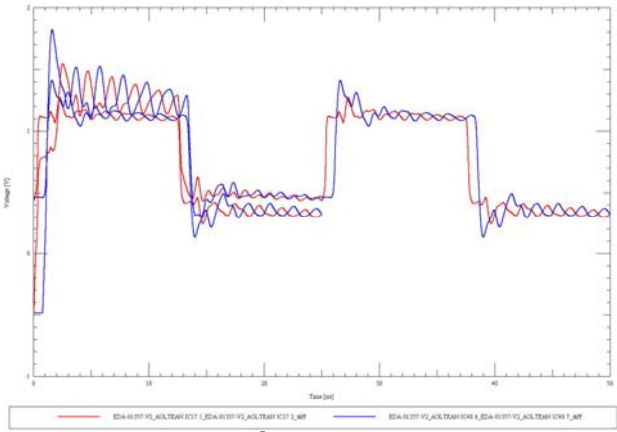
3 different paths: (1) BC1 (2) BCRef (3) BC2



Main_BC1



Main_BCRef



Main_BC2

Why does the path for BC2 look so different ?!

→SQ extracted another type of via for BC2 – why ? (under investigation with Cadence!)

Well, it might be an extraction error…

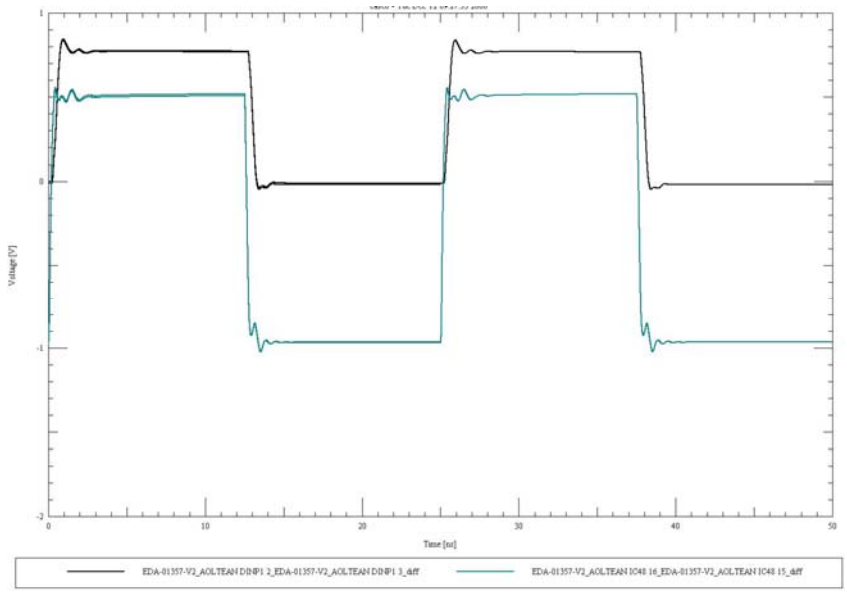
→Was it built a different via on the PCB for BC2 (I cannot see any difference from the Layout - see SQ_Via_Extraction.ppt)?

→ Do you see any anomalies in the measurements at this point (at the IC48 - signal Main_BC2)?

MC100EP57 = Interconnect = Delay25 [2]

Simulated path

MC100EP57 (IC48) = Interconnect = Delay25



➔how does the signal look like ?

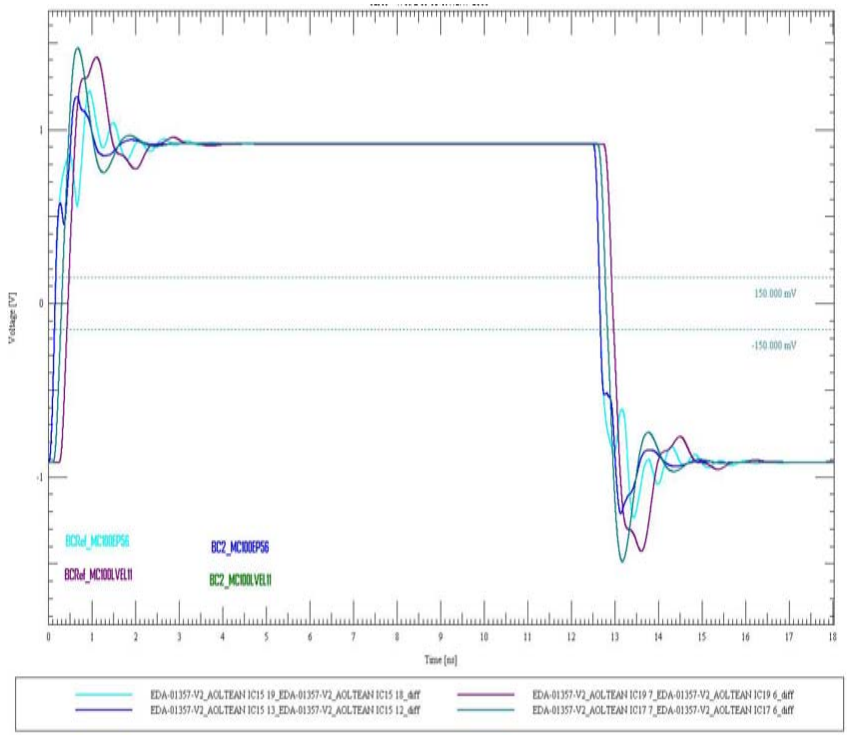
- unexpected shape for the BC2 for path [1]
- path [2] looks fine!

MC100EP56 = Interconnect = MC100LVEL11
BC2 compared to BCRef [1]

Simulated path
MC100EP56 = Interconnect = MC100LVEL11

BCRef
MC100EP56 (IC15)
MC100LVEL11 (IC19)

BC2
MC100EP56 (IC15)
MC100LVEL11 (IC17)



Comments
- Models used:
  - -IBIS for MC100EP56 and MC100LVEL11

➔ can we see any difference ?
No, not really. The waveforms for BC2 and BCRef look similar!

Conclusions

- The paths [MC100LVEL11 = Interconnect = DELAY25] for BC1, BC2 and BCRef seem to be fine
- The path [MC100EP57 = Interconnect = Delay25] is fine while the path [MC100LVEL11 = Interconnect = MC100EP57(IC48)] has a problem for BC2 which is under investigation (it might be just an extraction error!)
- The path [MC100EP56 = Interconnect = MC100LVEL11] seems to be fine as well

- So where did your jitter difference comes from ? For the moment I did not discover an error on your board layout which might cause the jitter on BCRef.
  - under investigation the difference we've seen for BC2 (see slide 6)
  - Might perform later on some crosstalk simulations on the board