USER MANUAL				
	Class: VME		Function: RF Optical Link (ANALOG)	
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RF_TX_A & RF_RX_A v1.0

Double Analog Optical Link VMEbus Interface Card and S/W

Summary:

This document describes the functionality of the RF_Tx_Analog and RF_RX_Analog card as well as the generic S/W that has been developed for it.

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1. INTRODUCTION

The RF_TX_A and RF_RX_A (RF to Optical and Optical to RF VMEbus cards) are interface cards developed as two channels analog Optical Link.

This link supports transmissions from 30 KHz to 3GHz in Analog (or digital) with a link gain of 5dB and with very low noise.

This document contains a hardware description of the boards and all the accessible registers of RF_TX_A and RF_RX_A cards as well as a description of the generic S/W that has been developed for monitoring these cards.

2. RF_RX AND RF_TX ANALOG HARDWARE

2.1. POWER DESCRIPTION

This board requires a VME crate with the standard VME64 power supply, with 12, -12, and 5 Volts available. The nominal consumption for these lines:

Voltage	Current (A)	Fuse Current
5V	120mA	Not fused
+12V	350mA/370mA	Not fused
-12V	70mA /9mA	Not fused

Table 2.1: Power consumption

In order to check the power supplied to the board, a four LEDs have been installed to indicate the presence of +12V*, -12V*, 5V and 3.3V

2.2. OPTICAL INTERFACES

The Optical interface is composed of 2 equal blocks based on two laser/photodiodes modules. These modules are compact modules without any control pin. That means that the optical to electrical conversion is achieve even if the VME interface is not set up.

MODULE	FUNTION
MITEQ LBT- 10K3G-13-23-P3	Laser Module
MITEQ LBT- 10K3G-15-23-10	Photodiode Module

Table 2.2: Modules and references

Each TX channel admits analog or digital input through a coaxial SMA connector and offers an Optical output through an E2000 APC connector for fast and accurate connection.

The TX and RX modules are in a metal receptacle with the only pins of Power and Monitor outputs that will help to know the intensity of the Laser or the signal received by the photodiode.

2.2.1. LINK CHARACTERISTICS

- The link is ready for single mode Fibre in 1330nm
- Link Gain: 5 dB (maximum Attenuation supported ~12dB)
- Analog Input / Output
- Bandwidth: 30KHz to 3Ghz
- Requires Heat sink with a proper airflow in order to avoid the destruction the components
- Laser Power: ~7dBm
- Receiver minimum sensibility ~ -8dBm

WARNING: the modules need or Heat sink or a constant airflow of at least 2m/s

2.3. VMEBUS INTERFACE

The VMEbus interface of the RF_Analog cards is implemented in its FPGA and based on a VHDL Module developed by the AB/RF group. This Module has been developed especially for VME64 but adapted for using some functionality of VME64X (like automatic addressing).

The firmware installed has been configured to work in the addressing mode of: A24/D16 and works as a memory decoder, where all the memory space is available.

The access modes (dictated by address modifier) are only available for 0x39 and 0x3D, where the there is no distinction between privilege user and normal user

From this 24bits of memory address, 6 bits are used for the module address [A23 to A18]. This address can be set up using the two rotary switches.

Picture 2.3: Module address selector

In addition, it is possible to fix automatically the module address by using the geographical address of VME64x.

In order to select the source of the module address (rotary switches or GEO addr.), from the 8 bits of the R.S. the 2 lower bits are designated to select it

2.3.1. ADDR MODULE SELLECTION

Address space available:

Note: M represent XXXX (any combination of 4 bits)

N represent XX (any combination of 2 bits)

0xM(N+0)0000 to 0xM(N+3) FFFF ➔ 256 Kbytes of memory

Rotary Switch 1	Rotary Switch 2	Module address (MA)
M	Bits(3:2)= N Bits(1:0)= "1 to 3"	Automatic GEO Address (5bits + 0)* [A23…A19] <= GEOGA(4 : 0) A18 <= 0
M	Bits(3:2)= N Bits(1:0)= "0"	0xMN Manual Address [A23…A20] <= M [A19…A18] <= N

**Requires VME64X crate*

Table 2.3.1: Address and ADDR Mode selection

In others words, the bottom rotary switch (sw1) controls the addressing mode with the lower two bits, which switches to automatic mode if the bit(0) or bit(1) = 1.

Examples:

Rotary Switch 1	Rotary Switch 2	Module MODO / ADDRESS / SPACE
0xF	0	Manual address Module address: 0xF0 0000 Board space: 0xF00000 to 0xF3 FFFF
0xF	1	Automatic address Module address: Depends on the slot into which the card is plugged
0xF	4	Manual address Module address: 0xF4 0000 Board space: 0xF40000 to 0xF7 FFFF

Table2.3.1.b: Examples of Module Addr

2.3.2. SOFTWARE: VME ADDRES MAP

Offset	Size (bytes)	Function	Mode	Remarks
0x0000	2	EDA ID	Read	0x1331 and 0x1332
0x0002	2	REF_POWER_COMPARATOR	Read/Write	16 bits, only 8 used
0x0004	2	CH1_ POWER	Read	16 bits, only 8 used
0x0006	2	CH2_ POWER	Read	16 bits, only 8 used
0x003A	2	BOARD ID (CERN ID)	Read	0x016E(RX) / 0x016F(TX)
>Others		Unused		

Table 2.3.2: VME Memory Map

2.3.3. REGISTERS DESCRIPTION

2.3.3.1. EDA IDENTIFICATION

Name	Offset	Size	Access
EDA ID	0x0000	16 bits	R

The card ID is just a register that can be used to identify the board… this default value is 0x1331 for the RF_Tx_A board and 0x1332 for the RF_RX board which correspond the EDA projects' numbers.

2.3.3.2. REFERENCE POWER THRESHOLD

Name	Offset	Size	Access	Def Rx	Def Tx
REF_POWER_COMPARATOR	0x0004	16 bits (8bits used)	R/W	0x0050	0x0020

The reference Power threshold is a register used as reference to be compared with the power that the laser is transmitting or the power arriving to the receiver. The result of the comparison is indicated in the front panel with a LED (Green light indicates power emitted/received > Power threshold, Red light indicates the opposite).

2.3.3.3. POWER MONITORING REGISTERS

Name	Offset	Size	Access
CH1_POWER	0x0004	16 bits (8bits used)	R
CH2_POWER	0x0006	16 bits (8bits used)	R

The data contained in this registers are obtained by the digitalisation of the signal generated by the optical modules.

The purpose of these registers is to evaluate and supervise the evolution of the lasers' power emissions and indicate if the laser or photodiode are transmitting or receiving any signal. At the same time, the result of the comparison between the threshold value and the power register is displayed in the front panel

In order to set up the threshold values, the user can be guided by the table 2.3.3.3b or with the equations described in the next section.

Board	Default Threshold Value	Meaning
RF_TX_A	0x50	4 dBm
RF_RX_A	0x20	-6.5dBm

Table 2.3.3.3b: Default Threshold Values

WARNING!!!! INVISIBLE LASER!!!!
THIS OPTICAL POWER CAN DAMAGE YOUR EYES. DO NOT LOOK DIRECTLY THROUGH THE FIBERS WHEN THE LASER IS ON OR USE APPROPRIATE EYE GLASSES

2.3.3.4. UNDERSTANDING THE POWER MONITOR

In order to understand and set up the default threshold values, the next measures have been done and these function obtained in approximation to the read values.

Board	Acq in Monitor Pin	Meaning
RF_TX_A	0x95	7dBm (0.034mw/Unit) (Measured)
RF_RX_A	0x1C	Dark
RF_RX_A	0x2B	1.3 dBm (1.4mW)
RF_RX_A	0x5F	7dBm (5mW)

Table 2.3.3.3a: Power Monitor Measurements

$$P(Tx_{mW}) = (Pwread) * 0.034mW / unit$$

$$P(Rx_{mW}) = (Pwread - 0x1C) * 0.082mW / unit$$

2.3.3.5. BOARD IDENTIFICATION

Name	Offset	Size	Access
BOARD ID	0x003A	16 bits	R

The card ID is just a register that can be used for identify the board. This register is situated in offset 0X003A. Its normal value is 366 and 367(decimal) for RX and TX Respectively, and they correspond to the ESS board numbers.

2.4. BOARD CONFIGURATION JUMPERS AND SWITCH (RX AND TX)

Element	Description
LSB rotary switch	See Table x
MSB rotary switch	See Table x
Reset(Front Panel) push button	Generate a Soft reset of the FPGA when is pressed
ST5	Always ON
ST4	Always OFF
ST1	Frequency selector0 for the JTAG
ST2	Frequency selector1 for the JTAG
ST3	If ST3 is ON -> the FPGA will be reprogrammed when the VME crate reset will be activated (SysReset)

Table 2.4: Jumpers and Switch descriptions

2.5. FIBRE / CABLE CONNECTIONS TX

Connector name	To be connected to	Format
CH1 out Optical Link	RF Analog RX	Optical: As RF input (signal Inverted)
CH1 RF In	50omhs source	Analog or Digital
CH2 Out Optical Link	RF Analog RX	Optical: As RF input (signal Inverted)
CH2 RF In	50omhs source	Analog or Digital
J4	JTAG	JTAG MODE (FPGA)
J3	JTAG	BIT BLASTER MODE (EEPROM)

Table 2.5: Connectors and Descriptions in Tx

2.6. FIBRE / CABLE CONNECTIONS RX

Connector name	To be connected to	Format
CH1 In Optical Link	RF Analog TX	Optical
CH1 RF Out	50omhs load	Same format as Optical
CH2 In Optical Link	RF Digital TX	Optical
CH2 RF Out	50omhs load	Same format as Optical
J4	JTAG	JTAG MODE (FPGA)
J3	JTAG	BIT BLASTER MODE (EEPROM)

Table 2.6: Connectors and Descriptions in Rx

2.7. FRONT-PANEL LEDS RX AND TX

LED	Description
VME COMM	Indicates if the last communication was successful or wrong
CH1 LED	Green Indicates Power Transmitted/Received > Threshold
CH2 LED	Green Indicates Power Transmitted/Received > Threshold

Table 2.7: Front Panel LEDS

2.8. REFERENCES OR MORE INFORMATION

Lasers and Photodiodes evaluation (by Angel Monera)

RF_TX_A EDA documents (https://edms.cern.ch/nav/eda-01331)

RF_RX_A EDA documents (https://edms.cern.ch/nav/eda-01332)

Miteq Evaluation (by S.Baron and A.Monera)

Laser and Photodiodes Evaluation (by S.Baron and A.Monera)

3. TTC COMMON SOFTWARE

3.3. INTRODUCTION

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3.3.2. S/W ENVIRONMENT

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3.4. TEST PROGRAMS

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3.5. THE USER LIBRARY