Specifications for the TX/RX VME modules in the 10 kHz-3 GHz Analog Fiber optic link.

Dual TX module

1. **General description:** 160 mm wide, 6U-4TE VME module with 2 fiber optic Transmitters MITEQ LBT-10K3G-13-23-P3
2. **Size:** 160 mm wide, 6U, 4TE. Caution: **the 4TE width must not be exceeded**. This includes the required heat sink.
3. **Functionalities:**
    a. **RF and Optical:** two independent channels with SMA RF input and E2000APC Optical output. The transmitter is meant to be used with the companion MITEQ LBR-10K3G-15-23-10 module. The link characteristics are: (all performances measured with a fiber introducing 5 dB optical loss)
        i. RF frequency range: 10 kHz to 3 GHz
        ii. Gain: 0 dB (+- 1.5 dB typ.)
        iii. 1 dB compression at input: +3 dBm min @400 MHz
        iv. Noise Figure @ 400 MHz: 27 to 29 dB typ.
        v. Output noise spectrum limited to ~3 GHz (noise BW limiting at RX output)
        vi. VSWR in/out: 2.0:1 max (50 ohms)
        vii. RF connectors (in/out): SMA female/SMA female
        viii. Optical connectors: pigtail terminated in E2000 APC
        ix. Supply voltages: +- 12 V as standard LBL
        x. EMI filters on power supply lines
        xi. Photocurrent monitoring: same as standard LBL
        xii. Case: same as standard LBL
        xiii. All other parameters same as standard 3 GHz LBL

    Specs for standard LBL modules are http://www.miteq.com/micro/fiberoptics/d294/spec.html
    b. **Controls:** LBR-10K3G-15-23-10 has a **Photocurrent Monitor pin** that provides an analog signal related to the optical power. This signal will be converted with an ADC and stored into an *Optical Power* register (16 bits word) that can be read via the VME interface (J1 connector). A 16 bits *Optical Threshold* register can be read/written via the VME interface. The comparison between *Optical Power* and *Optical Threshold* will set a bit in a *Status* register. A two-colors LED on the front panel will be set accordingly.
4. **Connectors:**
    a. **RF in (2x):** the Optical Transmitter has a female SMA input that must be routed to the front panel with a short semi-rigid cable (SUHNER Sucoform 141-50 or equivalent see http://www.hubersuhner.com/products/hs-p-rf.htm) with SMA male connector SUHNER 11 SMA-50-3-15 on the TX side and SMA straight bulkhead cable jack SUHNER 24 SMA-50-3-15 on the front panel.
    b. **Optical Out (2x):** the TX pigtail (terminated in an E2000 APC) connector will be routed to an optical feed through on the front panel. Care will be taken to protect the pigtail.
    c. **VME J1 connector:** the +- 12 V DC power supply come from the J1 (3x32 pins) connector. The VME access is done in A24/D16 format. The extended format is NOT used.
    d. **J2 connector:** the bottom 3x32 bits connector is not used. All pins are left floating.
5. **LED:Optical Power Out (2x):** a two-colors LED on the front panel indicates that the TX output power is OK (green) or too low (red). The threshold is set via the *Optical Threshold* register mentioned in 3.b

6. **Power supply:** The +- 12 V will be filtered/regulated on the card to reduce the glitches from the switched-mode power supplies. EMI filter (such as TUSONIX 4701-001, see http://www.tusonix.com/smt.html) will be inserted on the supply lines, close to the TX.
7. **Cooling:** the TX must be placed on a heat sink. The forced air flow is vertical bottom to top, 1 m/s minimum speed. CAUTION: the total width (with heat sink) must not exceed the size of a 4TE module.
8. **Front panel:** ATOS, 6U, 4TE, avec poignee extracteurs hyperrack, Alodine 1500.
9. **Design tools:** The FPGA will be designed with *Visual Elite.* (The VME interface can be provided by AB/RF. Interface with a multi-channel serial ADC (MAX1270) is also available (eda-00331 on edms). Contact John Molendijk). Schematics will be designed with *Cadence*. Layout will be done at the CERN Design Office EST/DEM. Cadence files and documentation will be stored in edms with an eda number

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Dual RX module

1. **General description:** 160 mm wide, 6U-4TE VME module with 2 fiber optic Transmitters MITEQ LBR-10K3G-15-23-10
2. **Size:** 160 mm wide, 6U, 4TE. Caution: **the 4TE width must not be exceeded**. This includes the required heat sink.
3. **Functionalities:**
    a. **RF and Optical:** two independent channels with E2000APC Optical input and SMA RF output. The receiver is meant to be used with the companion MITEQ LBT-10K3G-13-23-P3 module. The link characteristics are described above.
    Specs for standard LBL modules are http://www.miteq.com/micro/fiberoptics/d294/spec.html
    b. **Controls:** LBT-10K3G-13-23-P3 has a **Photocurrent Monitor pin** that provides an analog signal related to the detected optical power (carrier). This signal will be converted with an ADC and stored into an *Optical Power* register (16 bits word) that can be read via the VME interface (J1 connector). A 16 bits *Optical Threshold* register can be read/written via the VME interface. The comparison between *Optical Power* and *Optical Threshold* will set a bit in a *Status* register. A two-colors LED on the front panel will be set accordingly.
4. **Connectors:**
    a. **RF out (2x):** the Optical Receiver has a female SMA input that must be routed to the front panel with a short semi-rigid cable (SUHNER Sucoform 141-50 or equivalent see http://www.hubersuhner.com/products/hs-p-rf.htm) with SMA male connector SUHNER 11 SMA-50-3-15 on the RX side and SMA straight bulkhead cable jack SUHNER 24 SMA-50-3-15 on the front panel.
    b. **Optical In (2x):** the RX pigtail (terminated in an E2000 APC) connector will be routed to an optical feed through on the front panel. Care will be taken to protect the pigtail.
    c. **VME J1 connector:** the +12 V DC power supply comes from the J1 (3x32 pins) connector. The VME access is done in A24/D16 format. The extended format is NOT used.
    d. **J2 connector:** the bottom 3x32 bits connector is not used. All pins are left floating.
5. **LED:Optical Power In (2x):** a two-colors LED on the front panel indicates that the RX detected power is OK (green) or too low (red). The threshold is set via the *Optical Threshold* register mentioned in 3.b
6. **Power supply:** The +12 V will be filtered/regulated on the card to reduce the glitches from the switched-mode power supplies. EMI filter (such as TUSONIX 4701-001, see http://www.tusonix.com/smt.html) will be inserted on the supply lines, close to the RX.
7. **Cooling:** the RX must be placed on a heat sink. The forced air flow is vertical bottom to top, 1 m/s minimum speed. CAUTION: the total width (with heat sink) must not exceed the size of a 4TE module.

8. **Front panel:** ATOS, 6U, 4TE, avec poignee extracteurs hyperrack, Alodine 1500.
9. **Design tools:** The FPGA will be designed with *Visual Elite.* (The VME interface can be provided by AB/RF. Interface with a multi-channel serial ADC (MAX1270) is also available (eda-00331 on edms). Contact John Molendijk). Schematics will be designed with *Cadence*. Layout will be done at the CERN Design Office EST/DEM. Cadence files and documentation will be stored in edms with an eda number.